



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,291	02/26/2002	Takayuki Tamura	XA-9638	5343
181	7590	11/04/2004		
MILES & STOCKBRIDGE PC 1751 PINNACLE DRIVE SUITE 500 MCLEAN, VA 22102-3833			EXAMINER ABRAHAM, ESAW T	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/082,291	Applicant(s) TAMURA ET AL.	
	Examiner Esaw T Abraham	Art Unit 2133	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 February 2002.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) <i>p</i>                                   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Claims **1-18** are presented for examination.

#### ***Priority***

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

#### ***Claim objections***

3. Claims 1 and 10 are objected to because of the following informalities:
  - a) Please change the term "capable of" to "configured for" in claim 1 line 4.
  - a) Please change the term "capable of" to "configured for" in claim 10 lines 2 and 10.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
4. Claims **1-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohara (U.S. PN: 5,724,285).

As per claim 1, Shinohara in figure 3 teaches or disclose a card (21) comprise a flash memory controller (28) for controlling a flash memory (24). The flash memory controller (28), in a memory control (23) connected to an outside or host computer (22) to access instruction and a process for adding an error correction code by an ECC circuit (31) to data, which is written to the flash memory (24) from the host computer (22). Shinohara further teaches that the card comprising an error correcting code circuit, wherein the controller reads data in flash memory device through said error correcting code circuit and writes corrected data in a portion in which said error correcting code circuit detects a correctable read error when data stored in flash memory device are refreshed (see claim 2). Shinohara **does not explicitly teach** a memory controller controls a process for conducting an error detection and correction process to non-volatile memory by using an ECC code independently of the process. **However**, Shinohara teaches that the controller reads data in a flash memory device through the error correcting code circuit and writes corrected data on which the error correcting code circuit detects correctable read errors when data stored in the flash memory device are refreshed (see col. 2, lines 51-56), which Shinohara's memory controller is basically functioning the same as the applicant's invention when controlling the flash memory. **Therefore**, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to conduct an error detection and correction process when reading out data from the non-volatile (flash) memory. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to in order to improve the reliability of the memory card.

As per claims 2 and 9, Shinohara teaches or discloses all the subject matter claimed in claim 1 including Shinohara teaches that the controller reads data in the flash memory device

Art Unit: 2133

through the error correcting code circuit and writes corrected data on which the error correcting code circuit detects correctable read errors when data stored in the flash memory device are refreshed (see col. 2, lines 51-56). Further, Shinohara teaches that the flash memory controller is connected to the flash memory for controlling data write and data read to and from the flash memory (see col. 4, lines 12-16)

As per claim 3, Shinohara teaches or discloses all the subject matter claimed in claim 1 including Shinohara teaches that the controller reads data in the flash memory device through the error correcting code circuit and writes corrected data on which the error correcting code circuit detects correctable read errors when data stored in the flash memory device are refreshed (see col. 2, lines 51-56). Further, Shinohara teaches that the flash memory controller is connected to the flash memory for controlling data write and data read to and from the flash memory (see col. 4, lines 12-16). Furthermore, Shinohara teaches a controller, coupled to said flash memory device and a timer, which refreshes data stored in said flash memory device if said timer has counted the predetermined time when the external power supply is started again (see claim 1).

As per claim 4 and 5, Shinohara teaches or discloses all the subject matter claimed in claim 1 including Shinohara teaches that the controller reads data in the flash memory device through the error correcting code circuit and writes corrected data on which the error correcting code circuit detects correctable read errors when data stored in the flash memory device are refreshed (see col. 2, lines 51-56). Further, Shinohara teaches a controller, coupled to said flash memory device and a timer, which refreshes data stored in said flash memory device if said timer has counted the predetermined time when the external power supply is started again (see claim 1).

As per claims 6-8, Shinohara teaches or discloses all the subject matter claimed in claim 1 including Shinohara teaches a memory cell in a flash memory comprises a memory transistor of double gate structure consisting of a control gate and a floating gate and a flash memory stores a data according to a change in threshold value of the transistor by injecting or extracting electrons to and from a floating gate insulated electrically (see col. 1, lines 37-50) and further Shinohara teaches that the PC card comprises an error correcting code circuit and the controller reads data in the flash memory device through the error correcting code circuit and writes corrected data on which the error correcting code circuit detects correctable read errors when data stored in the flash memory device are refreshed (see col. 1, lines 50-55).

5. Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohara (U.S. PN: 5,724,285) in view of Beppu (U.S. PN: 6,256,762).

As per claim 10, Shinohara teaches all the subject matter claimed in claim 1 including a memory controller comprising a host interface circuit (see fig. 3, element 25), a flash memory controller (28) and ECC circuit (31). Shinohara **does not explicitly teach** or disclose a memory interface circuit connectable to the non-volatile (flash memory) memory. **However**, Beppu in an analogous art teaches a non-volatile memory (EEPROM) capable of realizing error correction at high speed (see col. 2, lines 49-52) and further, Beppu in figure 1 teaches that a memory interface part (17) connected to the flash memory (see col. 5, lines 38-42). **Therefore**, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to combine (incorporate) the memory interface circuit of Beppu into Shinohara's memory card for constructing a memory part and for executing the reception of data read from the memory part by the disk controller (3). **This modification** would have been obvious because a

Art Unit: 2133

person having ordinary skill in the art would have been motivated to do so in order to provide a method for correcting and detecting having a high reliability.

As per claims **11 and 12**, Shinohara in view of Beppu teach all the subject matter claimed in claim 10 including Shinohara in figure 5 teaches a control circuit (48) connected to the power supply (57) through flash memory (44).

As per claims **13 and 14**, Shinohara in view of Beppu teach all the subject matter claimed in claim 10 including Shinohara teaches that the controller reads data in the flash memory device through the error correcting code circuit and writes corrected data on which the error correcting code circuit detects correctable read errors when data stored in the flash memory device are refreshed (see col. 2, lines 51-56). Further, Shinohara teaches a controller, coupled to said flash memory device and a timer, which refreshes data stored in said flash memory device if said timer has counted the predetermined time when the external power supply is started again (see claim 1). Furthermore, Shinohara teaches flash PC card has a control circuit for reading or writing data to and from the flash memory according to a request of data read or data write from an information processor connected to the card (see col. 1, lines 12-19).

As per claims **15 and 16**, Shinohara in view of Beppu teach all the subject matter claimed in claim 10 including Shinohara that flash PC card has a control circuit for reading or writing data to and from the flash memory according to a request of data read or data write from an information processor connected to the card (see col. 1, lines 12-19).

As per claim 17, Shinohara in view of Beppu teach all the subject matter claimed in claim 10 including Shinohara that flash PC card has a control circuit for reading or writing data to and from the flash memory according to a request of data read or data write from an information

Art Unit: 2133

processor connected to the card (see col. 1, lines 12-19). Further, Shinohara in figure 1 teaches that the flash memory controller (8) is connected to the flash memory 4 for controlling data write and data read to and from the flash memory (4) and when the host requests data read of data in a logical sector through the interface (5), the microprocessor (6) reads data in a physical sector in correspondence to the logical sector determined by the address conversion circuit (9).

As per claim 18, Shinohara in view of Beppu teach all the subject matter claimed in claim 10 including Shinohara in figure 5 element 51 teaches an ECC circuit.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6185134 Tanaka

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



Esaw Abraham

Art unit: 2133



Art Unit: 2133

②  
GUY J. LAMARRE  
PRIMARY EXAMINER